Improved Deep Trench Structure and Memory Device Having the Same

BACKGROUND OF THE INVENTION

1.Field of the Invention

The present invention relates to a semiconductor memory device, more specifically, to a deep trench structure facilitating electrical test.

2. Description of the Prior Art

In semiconductor technology, testing technique is used to detect the defects and bugs in the wafers in order to find out defective products and promote the throughput. The electrical test for the semiconductor memory device is very important. The electrical parameters of the memory device directly influence the function and performance of the memory.

In the current techniques for semiconductor memory devices, deep trench technique is generally used in a semiconductor memory device structure having compact memory cell array. Because of the buried straps in the structure, it is impossible to directly access the deep trench capacitor. Accordingly, it is difficult to measure the leakages at the buried strap side such as gate inducing drain leakage (GIDL) and junction leakage.

Therefore, there is a need for a solution to overcome the problems stated above. The present invention satisfies such a need.

SUMMARY OF THE INVENTION

An objective of the present invention is to provide a deep trench structure of semiconductor device, which facilitates the measurement of the leakage currents.

Another objective of the present invention is to provide a semiconductor memory device, in which the leakage currents are easy to measure.

According to an aspect of the present invention, a deep trench structure of semiconductor device is characterized in that the cross section of the deep trench communicates with two different active areas of the semiconductor device.

According to another aspect of the present invention, a semiconductor memory device comprises a plurality of bit lines, each bit line is adjacent to each other; ~~a plurality of gates~~

~~crossing with said bit lines;~~ a plurality of active areas, ~~each of which is connected with one of said bit lines~~ a first active area is connected with a bit line and a second active area is connected with another bit line, these two bit lines are adjacent to each other, and each active area having two cells; a plurality of word lines, each word line is connected with one cell; and a plurality of deep trenches, ~~at least~~ one of which ~~has a cross section~~ communicate~~sing~~ with one of the two cells located in the first active area and one of the two cells located in the second active area ~~different active areas~~, so as to measure a leakage current between the first and the second active areas.

BRIEF DESCRIPTION OF THE DRAWINGS

The following drawings are only for illustrating the mutual relationships between the respective portions and are not drawn according to practical dimensions and ratios. In addition, the like reference numbers indicate the similar elements.

Fig. 1 shows a schematic diagram of the top view of a portion of a semiconductor memory device having a deep trench structure in accordance with the present invention; and

Fig. 2 shows the longitudinal sectional diagram taken from the ~~path~~ cross-section line A-A in Fig. 1.

DETIALED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the present invention will be described in detail with reference to the accompanying drawings.

With reference to Fig. 1, it is a schematic diagram showing a top view of a portion of a semiconductor memory device having deep trenches in accordance with the present invention. Reference numbers 11a and 11b indicates a bit line, 12 indicates a word line~~gate crossing with said bit line,~~. ~~and t~~The bit lines 11a and 11a are adjacent to each other; and ~~gates~~ the bit lines 11a and 11b and the word lines 12 constitute an array arrangement. Reference numbers 13, 13' and 13" indicate active areas, active area 13' is connected with the bit line 11a and active areas 13 and 13 are ~~connected~~ with the bit lines 11b.~~,~~ Reference number 14

indicates a conventional deep trench, while 15 indicates a deep trench in accordance with the present invention. A source S, a gate G, and a drain D together form a cell in the present invention, according to this, there are two cells in each of the active areas 13, 13', and 13", and each cell is connected to a word line 12. Generally, bit line contact windows 16, 16', and 16" are placed respectively in the active areas 13, 13', and 13" in order to connect with the later developed bit lines 11a and 11b.–

As shown in the drawing, the cross sections of the deep trenches 15 are lengthened, so that the two deep trenches 15 respectively communicate with– one of the two cells located in active area 13 and one of the two cells located in active area 13'~~active areas 13 and 13'~~, as well as one of the two cells located in active area 13" and one of the two cells located in active area 13'~~active areas 13" and 13' connected with adjacent bit lines~~. By means of such a structure, GIDL current and junction leakage current can be easily measured through the ~~gate~~ word line 12~~.~~, for instance, the bit line contact windows 16, 16', and 16" are used to measure the leakage currents from the deep trench 15 to the bit lines 11a and 11b, from the deep trench 15 to the substrate, from the deep trench 15 to the buried strap (not shown), and from the deep trench 15 to the word lines 12.

Fig. 2 shows a schematic longitudinal sectional diagram taken from the path A-A in Fig. 1 for reference, wherein two dashed lines indicate the vertical cross-section line A-A shown in Fig. 1; ~~WL~~ G indicates a ~~word line~~gate~~.~~, the dotted regions S indicate the sources, the dotted regions D indicate the drains; the regions 12 indicate the word lines, respectively control the two cells in one active area 13, 13', and 13". The shaded regions 16, 16', and 16" between the gates G are bit line contact window connecting with the bit line 11a or 11b, the shaded regions 18a and 18b are the insulators at the same layer, and blank regions 18c are the insulator at another layer, the horizontal shaded bars 19 are top trench oxide, the vertical shaded bars 20 are collar oxide, and structures 21 are buried plate.

While the embodiment of the present invention is illustrated and described, various

modifications and alterations can be made by persons skilled in this art. The embodiment of the present invention is therefore described in an illustrative but not restrictive sense. It is intended that the present invention may not be limited to the particular forms as illustrated, and that all modifications and alterations which maintain the spirit and realm of the present invention are within the scope as defined in the appended claims.

ABSTRACT

Disclosed is a deep trench structure for a semiconductor memory device. The deep trench in accordance with the present invention has a cross section communicating with two difference active areas, which are respectively connected to two adjacent bit lines of the semiconductor memory device.